Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE
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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES
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Ex parte SHIGERU TAKASAKI
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Appeal No. 1997-1637
Application 08/432,270[1]
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ON BRIEF
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Before URYNOWICZ, THOMAS and HAIRSTON, Administrative Patent Judges.

URYNOWICZ, Administrative Patent Judge.

DECISION ON APPEAL

This appeal is from the final rejection of claims 8-13, all the claims pending in the application.

The invention pertains to a logic circuit simulator. Claim 8 is illustrative and reads as follows:

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[1] Application for patent filed May 1, 1995. According to the appellant, the application is a division of Application 08/074,725, filed June 10, 1993, now Patent No. 5,572,708, issued November 5, 1996, which is a continuation of Application 07/486,705, filed February 28, 1990, now abandoned.

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A logic simulator for simulating a logic circuit defined by a plurality of sentences, each sentence being identified by an identifier and comprising at least one operator and at least two variables which are operated on according to said at least one operator, said logic simulator comprising:

an identifier memory for memorizing a plurality of identifiers each specifying one of said sentences, respectively;

a model memory for memorizing a plurality of operators which carry out operations specified by said sentences;

a variable memory for memorizing a plurality of initial values of the variables specified by said sentences;

a flag memory for memorizing a plurality of flags in correspondence with said sentences, each of said flags being indicative of whether or not said initial values of the variables specified by each of said sentences are changed during said simulation of said sentences;

a sentence calculating means connected to said identifier memory, said model memory, said variable memory, and said flag memory for carrying out calculation on one of said sentences at a time only when a change is indicated by one of said flags that corresponds to said one of said sentences, said sentence calculating means producing a result of said calculation based on at least one of said operators and at least two of said initial values of said variable, said at least one of said operators and said at least two of said initial values of said variables being specified by said one of said sentences;

a result memory for memorizing an initial result value; and substituting means connected to said result memory and said sentence calculating means for substituting said result of said calculation for said initial result value.

The reference relied upon by the examiner as evidence of

obviousness is:

Cocke et al. (Cocke)   4,306,286   Dec. 15,

1981

The appealed claims stand rejected under 35 U.S.C. § 103 as

being unpatentable over Cocke.

The respective positions of the examiner and the appellant
with regard to the propriety of the rejections is set forth in the
final rejection (Paper No. 6) and the examiner's answer (Paper No.
13) and the appellant's brief (Paper No. 12) and reply brief
(Paper No. 14).

<u>Appellant's Invention</u>

We agree with the examiner that the summary of the invention
contained in pages 2-5 of the brief is correct and we adopt it as
our own.

<u>The Rejection under 35 U.S.C. §103</u>

Appellant observes that claim 8 requires a sentence
calculating means for carrying out calculation on one of a
plurality of sentences at a time only when a change is indicated
by one of the flags stored in memory. The contention is made that
the examiner concedes that this feature is not taught by Cocke.

With respect to the above, the examiner takes the position at
pages 3 and 4 of his answer that,

Even [though] Cocke do not explicitly disclose sentence
calculating means for carrying out calculation on one of the
sentences as claimed, [a] practitioner in the art at the time the
invention was made would have found it obvious the computer would
distribute data and instructions to the simulator to perform the
simulation, and centrally control the computation of the

processors because Cocke disclose that the computer controls the processors [sic] operations by setting the reservation table (see Figs. 11, 12), sending simulation instruction and data to the processors, and the processors would simulate the instructions.

We will not sustain the rejection of claim 8.

It is considered that even though Cocke discloses that the basic processors of its logic simulation device may operate in combination with a host computer and a local computer (collectively, the examiner's central computer) which are used to provide loading functions and to analyze the results of a simulation, the examiner has not satisfied his burden of showing how the computer operation referred to by him satisfies the language of claim 8 requiring sentence calculating means "for carrying out calculation on one of said sentences at a time only when a change is indicated by one of said flags that corresponds to said one of said sentences". It is not apparent to us that the prior art structure would perform the above function.

In the final rejection at page 3, the examiner acknowledged that the flag settings of the claimed invention utilized to control calculation on sentences are different from flag settings of Cocke disclosed at column 8, lines 12-24. However, the examiner indicated it would have been obvious to logic designers to set up correct input values to logic functions in order to

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correctly simulate the logic functions. This position is not

persuasive either. It appears to presume that the flag settings

of Cocke are not correct and would not result in accurate gate

simulation of logic circuits, and that one of ordinary skill in

the art would have sought to change them so as to provide flags of

the type claimed by appellant so as to correctly simulate logic

functions. There is no evidence to support such a position.

      To the extent that the examiner may have misstated his

position and simply means that it would have been obvious to

modify the flags of Cocke so as to perform the function of

appellant's sentence calculating means, the examiner has provided

no convincing motivation for doing so. The motivation set forth

by the examiner at page 3 of the final rejection, that being to

correctly simulate logic functions, assumes that Cocke does not

correctly simulate such functions. There is no evidence to that

effect.

      The examiner rejected claim 12, the only other independent

claim, based "under the same rationale" as claim 8 due to the

similarities of the two claims. Whereas we have decided not to

sustain the rejection of claim 8, we will not sustain the

rejection of claim 12.

In view of our decision with respect to independent claims

8 and 12, we will not sustain the rejection of dependent claims 9-

11 and 13.

Although we will not sustain the rejection of claims 8-13

for the reasons given above, we agree with the examiner that Cocke

discloses identifier, model, variable, flag and result memories

such as recited in claim 8 for the reasons given in the answer.

We also agree with the examiner that Cocke teaches a simulation

device capable of simulating circuitry at a functional level.

Appellant has not drawn attention to any specific definition of

simulation at a functional level which is recognized in the art,

nor has appellant provided its own definition of the term. It is

considered that Cocke performs simulation at a functional level in

that Cocke simulates the function of gates, such as the NAND

function of the gates illustrated in Figure 2 of the reference.

<u>REVERSED</u>

STANLEY M. URYNOWICZ, JR.   )
Administrative Patent Judge   )
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) BOARD OF PATENT
JAMES D. THOMAS   )
Administrative Patent Judge   ) APPEALS AND
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KENNETH W. HAIRSTON   )
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